WHAT IS CLAIMED IS:

1. A semiconductor device in which a gate electrode of a MISFET formed on a semiconductor substrate is electrically connected to a well region under a channel of said MISFET,

wherein said MISFET is formed in an island-shaped element region formed on said semiconductor substrate, and

electrical connection between said gate electrode of said MISFET and the well region in said semiconductor substrate are electrically connected on side of the island-shaped element.

2. A device according to claim 1, wherein said gate electrode is composed of a metal material.

3. A semiconductor device, comprising:

a semiconductor substrate including an island-shaped element region composed of a lower structure and an upper structure formed on said lower structure and having a smaller cross-sectional area parallel to a surface of said substrate than that of said lower structure;

a gate insulating film formed on an upper surface of said upper structure of the element region;

a sidewall insulating film formed on said lower structure and a side surface of said upper structure of the element region; and

a gate electrode formed on an upper surface of

said gate insulating film, and an upper surface of said sidewall insulating film, and the gate is connected to lower structure of the element via capacitor insulators formed on sides of the lower structure.

4. A semiconductor device comprising:

a semiconductor substrate including an island-shaped element region comprised of a lower structure and an upper structure formed on said lower structure and having a smaller cross-sectional area parallel to a surface of said substrate than that of said lower structure;

a gate insulating film formed on an upper surface of said upper structure of the element;

a sidewall insulating film formed on an upper surface of said lower structure and on a side surface of said upper structure of the element; and

a gate electrode connected to an upper surface of said gate insulating film, an upper surface of said sidewall insulating film, and a side surface of said lower structure of the element.

5. A device according to claim 4, wherein said gate electrode is composed of a metal material.

6. A semiconductor device, comprising:

a semiconductor substrate including an island-shaped element region composed of a lower structure and an upper structure formed on said lower structure and having a smaller cross-sectional area

parallel to a surface of said substrate than that of said lower structure;

a gate insulating film formed on an upper surface of said upper structure of the element;

a gate electrode formed on said gate insulating film;

an sidewall insulating film formed on a side surface of said upper structure of the element region and a side surface of said gate electrode so as to have an upper surface lower than an upper surface of said gate electrode; and

a contact electrode formed on a side surface of said lower structure of the element region and a side surface of said element sidewall insulating film and electrically connected to the side surfaces of said gate electrode and said lower structure of the element.

7. A semiconductor device according to claim 6, wherein said gate electrode is composed of a metal material.

8. A semiconductor device comprising:

a semiconductor substrate including an island-shaped element region comprised of a lower structure and an upper structure formed on said lower structure and having a smaller cross-sectional area parallel to a surface of said substrate than that of said lower structure;

a gate insulating film formed on an upper surface

of said upper structure of the element;

a sidewall insulating film formed on a side surface of said upper structure of the element;

a capacitor insulating film formed on each of opposite sides of said lower structure of the element;

a gate electrode formed on said gate insulating film; and

a capacitor electrode formed on said capacitor insulating film and electrically connected to said gate electrode.

9. A semiconductor device according to claim 8, wherein said gate electrode and said capacitor electrode are composed of a continuously formed electrode material.

10. A device according to claim 8, wherein said gate electrode is formed from a metal material.

11. A semiconductor device in which a gate electrode of a MISFET formed on a semiconductor substrate is electrically connected to a well region under a channel of said MISFET,

wherein said MISFET is formed on part of a side surface of an island-shaped element region formed on said semiconductor substrate, and

electrical connection between said gate electrode of said MISFET and the well region in said semiconductor substrate is done on an upper surface of the island-shaped element are electrically connected.

12. A semiconductor device according to claim 11, further comprising two gate electrodes formed on opposite side of the island-shaped element region.

13. A semiconductor device according to claim 12, further comprising a source and drain formed to sandwich said each gate electrodes formed on said opposite sides of the island-shaped element.

14. A semiconductor device comprising:

a semiconductor substrate including an island-shaped element comprised of a lower structure and an upper structure formed on said lower structure and having a smaller cross-sectional area parallel to a surface of said substrate than that of said lower structure;

a pair of gate insulating films formed on opposing sides of said lower structure of the element region, respectively;

a sidewall insulating film formed on a side surface of said upper structure of the element region;

a gate electrode formed on said pair of gate insulating films, an upper surface of said sidewall insulating film, and an upper surface of said upper structure of the element region; and

source and drain regions formed on opposite side surfaces of said lower structure of the element region so as to sandwich said pair of gate insulating films,

wherein bottom surfaces of said source and drain

diffusion layers formed on side surfaces of the element region are in contact with each other.

15. A method of manufacturing a semiconductor device, comprising the steps of:

patterning a semiconductor substrate to form an island-shaped element region comprised of a lower structure and an upper structure formed on said lower structure and having a smaller cross-sectional area parallel to a surface of said substrate than that of said lower structure;

forming an insulating film in contact with a side surface of said upper structure and an upper surface of said lower structure of the element region;

forming a disposable gate in a region on said semiconductor substrate where a gate electrode is to be formed;

forming a source and drain in said upper structure of the element region;

forming an interlayer insulating film on both sides of the disposable gate on said semiconductor substrate to expose an upper surface of the disposable gate;

removing the disposable gate to form a gate groove;

forming a gate insulating film on an upper surface of said upper structure of the element region, the upper surface being exposed to a bottom surface of the

gate groove; and

forming a gate electrode buried in the gate groove and electrically connected to a side surface of said lower structure of the element region.

16. A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern in a region, where a source, drain, and channel of a MIS transistor are to be formed, on an upper surface of a semiconductor layer formed on stacked a semiconductor substrate and an insulating layer;

etching said semiconductor layer using said mask pattern as a mask to form a convex on said semiconductor layer;

forming a first sidewall insulating film on a side surface of said convex of said semiconductor layer;

etching said semiconductor layer using said mask pattern and said first sidewall insulating film as a mask to expose said insulating layer, thereby forming an island-shaped element region comprised of an upper structure formed from said convex and a lower structure formed under said upper structure;

forming a second sidewall insulating film on a side surface of said lower structure of the element region and a side surface of said first sidewall insulating film;

forming a disposable gate to cover a region, where

said gate electrode is to be formed, on upper surfaces of said insulating layer, said second sidewall insulating film, said first sidewall insulating film, and said upper structure of the element region;

forming said source and drain in said upper surface of said upper structure of the element region;

forming an insulating film to cover the disposable gate and planarizing an upper surface of said insulating film to expose an upper surface of the disposable gate;

removing the disposable gate to form a gate groove in which said side surface of said lower structure of the element region is exposed;

forming a gate insulating film on an upper surface of said upper structure of the element region on a bottom surface of the gate groove; and

forming a gate electrode buried in the gate groove.

17. A method of manufacturing a semiconductor device, comprising the steps of;

forming a mask pattern in a region on a semiconductor layer on a semiconductor substrate, where a source, drain, and channel of a MIS transistor are to be formed;

etching said semiconductor layer using said mask pattern as a mask to form a convex on said semiconductor layer;

forming a first sidewall insulating film on a side surface of said convex of said semiconductor layer;

etching said semiconductor layer using said mask pattern and said first sidewall insulating film as a mask to expose said insulating layer, thereby forming an island-shaped element region comprised of an upper structure formed from said convex and a lower structure formed under said upper structure;

forming an insulating layer to cover an upper surface of said semiconductor substrate outside the element region so as to expose an upper end portion of a side surface of said lower structure of the element region;

forming a second sidewall insulating film on a side surface of said lower structure of the element region and a side surface of said first sidewall insulating film;

forming a disposable gate to cover a region, where said gate electrode is to be formed, on upper surfaces of said insulating layer, said second sidewall insulating film, said first sidewall insulating film, and said upper structure of the element region;

forming said source and drain in said upper surface of said upper structure of the element region;

forming an insulating film to cover the disposable gate and planarizing an upper surface of said insulating film to expose the disposable gate;

removing the disposable gate to form a gate groove to expose said side surface of said lower structure of the element region;

forming a gate insulating film on an upper surface of said upper structure of the element region on a bottom surface of the gate groove; and

forming a gate electrode buried in the gate groove.

18. A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern in a region, where a source, drain, and a channel region of a MIS transistor are to be formed, on an upper surface of a semiconductor layer formed on stacked a semiconductor substrate and an insulating layer;

etching said semiconductor layer to a predetermined depth using said mask pattern as an etching mask to form a convex on said semiconductor layer;

forming an element sidewall insulating film on side surfaces of said mask pattern and said convex of said semiconductor layer;

etching said semiconductor layer using said mask pattern and said element sidewall insulating film as a mask to expose said insulating layer, thereby forming an island-shaped element region comprised of an upper structure formed from said convex and a lower structure formed under said upper structure;

forming a dummy contact on a side surface of said lower structure of the element region and a side surface of said element sidewall insulating film;

forming a first insulating film around the dummy contact;

recessing an upper surface of said element sidewall insulating film;

partially or completely removing said mask pattern;

forming a disposable gate connected to the dummy contact on an upper surface of a region where a gate electrode is to be formed, including the channel region of said upper structure of the element region;

forming said source and drain in said upper structure of the element region using the disposable gate as a mask;

forming a second insulating film on said semiconductor substrate to cover a side surface of the disposable gate and expose an upper surface of the disposable gate;

removing the disposable gate to form a gate groove in which the dummy contact is exposed;

forming a gate insulating film in the gate groove;

forming a gate electrode buried in the gate groove;

exposing the upper surface of the dummy contact;

removing the dummy contact to form a contact

trench in which said side surface of said lower structure of the element region is exposed; and

forming a contact electrode buried in the contact trench.

19. A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern in a region, where a source, drain, and channel region of a MIS transistor are to be formed, on a semiconductor substrate;

etching said semiconductor substrate to a predetermined depth using said mask pattern as an etching mask to form a convex on said semiconductor substrate;

forming a sidewall insulating film on side surfaces of said mask pattern and said convex;

etching said semiconductor layer using said mask pattern and said element sidewall insulating film as a mask to form an island-shaped element region comprised of an upper structure formed from said convex and a lower structure formed under said upper structure;

forming a dummy contact on a side surface of said lower structure of the element region and a side surface of said element sidewall insulating film;

forming a first insulating film around the dummy contact;

recessing an upper surface of said element sidewall insulating film;

partially or completely removing said mask pattern;

forming a disposable gate connected to the dummy contact on an upper surface of a region where a gate electrode is to be formed, including the channel region of said upper structure of the element region;

forming said source and drain in said upper structure of the element region using the disposable gate as a mask;

forming a second insulating film on said semiconductor substrate to cover a side surface of the disposable gate and expose an upper surface of the disposable gate;

removing the disposable gate to form a gate groove in which the dummy contact is exposed;

forming a gate insulating film in the gate groove;

forming a gate electrode buried in the gate groove;

exposing the upper surface of the dummy contact;

removing the dummy contact to form a contact trench in which part of a sidewall is connected to said side surface of said lower structure of the element region; and

forming a contact electrode buried in the contact trench.

20. A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern in a region on a semiconductor substrate, where a source, drain, and channel region of a MIS transistor are to be formed;

etching said semiconductor substrate to a predetermined depth using said mask pattern as a mask to form a convex on said semiconductor substrate;

forming a sidewall insulating film on side surfaces of said mask pattern and said convex;

etching said semiconductor layer using said mask pattern and said element sidewall insulating film as a mask to form an island-shaped element region comprised of an upper structure formed from said convex and a lower structure formed under said upper structure;

forming a disposable gate in a region on said semiconductor substrate, where a gate electrode is to be formed;

forming said source and drain in said upper structure of the element region;

forming an interlayer insulating film on said semiconductor substrate in contact with the sides of disposable gate to expose an upper surface of the disposable gate;

removing the disposable gate to form a gate groove in which the element region is partially exposed;

depositing an insulating film on an upper surface of the element region exposed to a bottom surface of the gate groove so as to form a gate insulating film on

said upper structure of the element region and form a capacitor insulating film on a side surface of said lower structure of the element region; and

burying an electrode pattern in the gate groove to form a gate electrode and capacitor electrode.

21. A method of manufacturing a semiconductor device, comprising the steps of:

forming a mask pattern in a region on a semiconductor substrate, where a source, drain, and channel region of a MIS transistor are to be formed;

etching said semiconductor substrate to a predetermined depth using said mask pattern as a mask to form a convex on said semiconductor substrate;

forming a sidewall insulating film on side surfaces of said mask pattern and said convex;

etching said semiconductor layer using said mask pattern and said element sidewall insulating film as a mask to form an island-shaped element region comprised of an upper structure formed from said convex and a lower structure formed under said upper structure;

forming a disposable gate in a region on said semiconductor substrate, where a gate electrode is to be formed;

forming said source and drain in a side portion of said lower structure of the element region;

forming an interlayer insulating film on said semiconductor substrate in contact with a side portion

of the disposable gate to expose an upper surface of the disposable gate;

removing the disposable gate to form a gate groove in which the upper surface of element region is partially exposed;

forming a gate insulating film on a side surface of said lower structure of the element region exposed to a bottom surface of the gate groove; and

forming a gate electrode buried in the gate groove.